REMARKS

Claims 1, 2, 5, 7, 9, 10, 15 and 17 have been amended. Claims 1 to 20 remain active in this application of which claims 5, 13 and 18 to 20 were allowed.

Claims 1 to 4, 6 to 12, and 14 to 17 were rejected under 35 U.S.C.103(a) as being unpatentable over the Benabes et al. article in view of the Chan article and Yamakido et al. or Voorman et al. The rejection is again respectfully traversed.

All of the rejected independent claims now require a pair of analog input currents with one of the input current being selected in response to the output of the digital signal from the quantizer. No such feature is taught or suggested b y any of the cited references.

It is also again noted, as stated from the inception, that the claims require that both the discrete time circuit and the continuous time circuit be passive. Clearly, Benabes nowhere teaches or suggests the circuit as claimed either in structure format or in method format other than stating that a design for a passive sigma-delta converter is provided. The claims herein require much more. Claim 1 requires the combination of "a passive discrete time circuit for receiving the digital feedback signal and an input signal, the input signal comprising information and one or more analog input currents; converting the digital feedback signal into an analog feedback signal during a first discrete time; and summing the analog feedback signal and the one or more analog input currents during a second discrete time to yield one or more summed signals" and "a passive continuous time circuit comprising a plurality of passive resistive and capacitive elements, the continuous time circuit coupled to the discrete time circuit to filter the one or more summed signals using a first first-order filter containing resistive and capacitive elements serially connected to a second first order filter containing resistive and

capacitive elements to form a second first order filter to generate one or more filtered signals, the first-order filters comprising one or more first passive elements of the plurality of passive elements". The examiner has directed attention to Fig. 3 of Benabes et al. However, this figure is merely a showing of a filter using all passive elements. Claim 1 calls for much more. Not only does claim 1 require the combination of filters as claimed, but, in addition, claim 1 requires "a passive discrete time circuit for receiving the a digital feedback signal and an input signal, the input signal comprising information and one or more analog input currents; converting the digital feedback signal into an analog feedback signal during a first discrete time; and summing the analog feedback signal and the one or more analog input currents during a second discrete time to yield one or more summed signals" coupled to the passive continuous time circuit. No such circuit is taught or suggested by Benabes et al. either alone or in the combination as claimed.

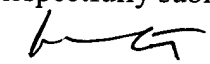
As to the Chen reference, while, as noted in the Office action, Benabes et al. refers to this publication, it is noted that the reference to Chen is with reference to "first order modulators" and nothing else. Clearly, Benabes et al. nowhere considered combining the circuit of Chen with their device. Furthermore, the circuit of Chen nowhere teaches or suggests the specific features of the discrete time circuit as claimed, even were it combinable with Benabes et al., which it clearly is not.

As to Voorman et al., there is clearly no teaching or suggestion to combine this reference with Benabes et al. and Chen other that from a first study of the subject disclosure.

In summary, as to each of the rejected independent claims, these claims require , in addition to the combination of the passive continuous time circuit in combination with a passive discrete time stage wherein the input signal and the feedback signal are combined, a pair of analog input currents with one of the pair being subbed with the feedback signal, the one being summed dependent upon the output digital signal from the digitizer. There is no teaching or suggestion in any of the references not only of such a circuit, but of such a combination. Even were the individual circuits to be depicted in the prior art, some of which are not, the combination as claimed is nowhere taught or suggested,

In view of the above remarks, favorable reconsideration and allowance are respectfully requested.

Respectfully submitted,



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